

Ruthwik Reddy Sunketa

623-275-8696 | rsunketa@asu.edu | [linkedin.com/in/rsunketa](https://www.linkedin.com/in/rsunketa)

SUMMARY

Computer Engineering PhD student specializing in FPGA architecture, design, and automated EDA flows. Current research focuses on next-generation FPGA architectures for AI/ML workload acceleration and hardware-software co-design. Experience in digital design, verification, physical design, and EDA flow development.

EDUCATION

Arizona State University

Ph.D. in Computer Engineering

Master's in Computer Engineering

Tempe, AZ

Aug 2025 – Present

Aug 2023 – July 2025

Relevant Coursework: Reconfigurable Computing, VLSI Design, Hardware Security and Trust, Advanced Hardware and Systems for Machine Learning, Statistical Machine Learning, Real-Time Digital Signal Processing

RESEARCH PROJECTS

ATLAS: Automated HLS for DL-Optimized FPGAs

March 2026 – Present

- Developed ATLAS, an automated ML-to-FPGA compilation flow that maps DL workloads onto FPGAs with custom hardblocks without manual RTL design or explicit hardblock instantiation
- Extended hls4ml to lower supported layers into architecture-agnostic GEMM calls; built a GEMM IP generator that composes FPGA hardblocks into arbitrary-shape GEMM IPs and integrates them into HLS as RTL blackboxes
- Evaluated ATLAS across 11 designs on a Tensor Slice-based FPGA, attaining 89% of hand-written RTL compute-area efficiency, a 24% improvement over soft-logic hls4ml, while reducing implementation effort from weeks to hours

3.3/5V Configurable Voltage FPGA

Aug 2025 – Jan 2026

- Explored mixed-voltage FPGA architectures with on-chip Digital LDOs (DLDOs) for drop-in replacement of legacy 3.3/5 V ICs
- Designed and evaluated a custom FPGA fabric using OpenFPGA, including architecture selection, scalable fabric generation, and bitstream-based functional verification
- Performed RTL-to-GDS physical design using OpenLane, including power analysis, DLDO sizing, DRC/LVS sign-off, and tapeout submission on SKY130 technology

OpenFPGA-NoC: Automated Fabric and Bitstream Generation for NoC-based FPGAs

Aug 2024 - June 2025

- Extended OpenFPGA framework to support hardened Network-on-Chips (NoCs) with arbitrary physical topologies
- Developed a dedicated NoC bitstream generator and configuration mechanism to manage dynamic compile-time address translation and global routing mode selection
- Evaluated NoC-based architectures through an automated RTL-to-bitstream flow, confirming a 3.66× frequency gain and 15% lower routing congestion for I/O-intensive workloads over traditional fabrics

PUBLICATIONS

- [1] Ruthwik Sunketa and Aman Arora, *ATLAS: Automated HLS for DL-Optimized FPGAs*, FPT, 2026. [Poster, Accepted]
- [2] Jiajun Hu, Ruthwik Reddy Sunketa, Lei Zhao, Archit Gajjar, Luca Buonanno, and Aman Arora, *NIFA: Nonlinear IMC Enhanced FPGA for Efficient ML Inference*, FPL, 2026. [Conference]
- [3] Ruthwik Reddy Sunketa, Jeevesh Choudhury, Aman Arora, *Programming Domain-Specific FPGA Hardblocks from HLS: An RTL Blackbox Approach*, RAW-IPDPS, 2026. [Workshop]
- [4] Archit Gajjar, Ruthwik Reddy Sunketa, Lei Zhao, Omar Eldash, Aishwarya Natarajan, Giacomo Pedretti, Aman Arora, Paolo Faraboschi, Jim Ignowski, and Luca Buonanno, *Azure-Lily: An FPGA Architecture with Analog IMC Engines for Efficient AI*, ACM TACO, 2026. [Journal]
- [5] Ruthwik Reddy Sunketa and Aman Arora, *Closing the Loop on FPGA Verification: An Iterative Framework for Maximizing Routing Resource Coverage*, ACM ISFPGA, 2026. [Poster]
- [6] Ruthwik Reddy Sunketa, Muhammad Ali Farooq, Ganesh Gore, Allen Boston, Pierre-Emmanuel Gaillardon, and Aman Arora, *OpenFPGA-NoC: Automated Fabric and Bitstream Generation for NoC-based FPGAs*, ACM TRETTS, 2025. [Journal]

TECHNICAL SKILLS

Programming: Python, C, C++, Verilog, SystemVerilog, Embedded C

Technologies: Quartus & Xilinx FPGA tools, Synopsys tools (VCS, Design Compiler, PrimeTime), Cadence tools (Genus, Innovus, Virtuoso), Open-source EDA tools (VTR/VPR, OpenFPGA, OpenROAD/OpenLane, Yosys)

ADDITIONAL EXPERIENCE

Teaching Assistant: CEN 598 - **Advanced Digital Design and Verification**, ASU

Summer 2025 and Fall 2026

Teaching Assistant: CSE 325 - **Embedded Microprocessor Systems**, ASU

Fall 2024

Intern: Systems Validation - **Medtronic**, Hyderabad, India

Spring 2023